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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER
TRAN, MICHAEL THANH

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/076,486	Applicant(s) CASPER ET AL.	
	Examiner Michael T Tran	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *February 19, 2002 through May 5, 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-32,40-49 and 56* is/are allowed.

6)☒ Claim(s) *1-5,12,13,33,34,50,51 and 57* is/are rejected.

7)☒ Claim(s) *6-11,35-39 and 52-55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. In response to the Communications dated February 19, 2002 through May 05, 2003, claims 1-57 are active in this application as a result of the addition of claim 57.

Election

2. Further review of the claims finds that there exists a generic claim. Therefore, the restriction requirement has been withdrawn.

Information Disclosure Statement

3. The information disclosure statement filed July 15, 2002 and September 26, 2002 has been considered. It is noted that the disclosures are duplicate hence there is only one signed copy being attached to this Office Action.

Claim Objections

4. Claims 6-11, 35-39, and 52-55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

It appears that the phrase "said element" of line 5 of claim 57 lacks antecedent basis.

Claim Rejections – 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1-5, 12, and 13 are rejected under 35 U.S.C 102(e) as being anticipated by Cowles et al. [U.S. Patent #6,449,203].

With respect to claim 1, Cowles et al. discloses a method of sensing a stored value of a programmable conductor random access memory element, the method comprising: precharging a digit line [D] and a digit complement line [*D] to a predetermined voltage value [*DVC2 – see the 2nd paragraph of the "Background of the Invention" section*]; activating an access transistor [50] coupled between said element and said digit line to apply a read voltage to said element [*see 6th paragraph of the "Detailed Description of the Invention" section*]; and comparing the voltage on said digit line with a voltage on said digit complement line to determine a logical state of said element [*see the 2nd paragraph of the "Background of the Invention" section*].

With respect to claim 2, Cowles et al. discloses, in the 2nd paragraph of the "Background of the Invention" section, that the act of precharging comprises precharging said digit line and said digit complement line to approximately Vdd [DVC2].

It is interpreted that Vdd is just a designated label without any numerical value associated to it.

With respect to claim 3, Cowles et al. discloses, in the 1st paragraph of the "Detailed Description of the Invention" section, that the act of precharging comprises receiving a precharge control signal at a precharge circuit [via controller 24 of figure 1] and coupling said digit line and said digit complement line to approximately Vdd [DVC2 - see, the 2nd paragraph of the "Background of the Invention" section]. It is interpreted that Vdd is just a designated label without any numerical value associated to it.

With respect to claim 4, Cowles et al. discloses, in the 2nd paragraph of the "Detailed Description of the Invention" section, that the act of precharging further comprises equilibrating said voltage on said digit line and said voltage on said digit complement line [via sense circuit [0]].

With respect to claim 5, Cowles et al. discloses, in the 2nd paragraph of the "Detailed Description of the Invetion" section, that the act of activating comprises firing a rowline [WORDLINES] coupled to a gate of said access transistor.

With respect to claim 12, Cowles et al. discloses that the method further comprising applying a voltage to a second terminal of said memory element, said voltage being between 0v and said predetermined voltage [Vcc].

With respect to claim 13, Cowles et al. discloses that the act of applying comprises applying said voltage to a cell plate [capacitor 54 has upper and lower plates] ties to said second terminal of said memory element.

7. Claims 33-34 are rejected under 35 U.S.C 102(e) as being anticipated

by Cowles et al. [U.S. Patent #6,449,203].

With respect to claim 33, Cowles et al. discloses, in figure 1, a semiconductor memory structure comprising: a digit line [D] and a digit complement line [D*]; a circuit for precharging [24] said digit line and said digit complement line to a predetermined voltage value [DVC2] prior to a read operation; an access transistor [50] for coupling a programmable conductor memory element [54] to said digit line during a read operation; and a sense amplifier [0] for comparing voltages on said digit line and said digit complement line during said read operation to determine a logical state of said memory element [see *the 2nd paragraph of the "Background of the Invention" section]*.

With respect to claim 34, Cowles et al. discloses that the predetermined voltage is approximately Vdd [DVC2]. It is interpreted that Vdd is just a designated label without any numerical value associated to it.

8. Claims 50-51 are rejected under 35 U.S.C 102(e) as being anticipated by Cowles et al. [U.S. Patent #6,449,203].

With respect to claim 50, Cowles et al. disclose, in figures 1 and 5, a processor system, comprising: a processor [see description of figure 5]; and a semiconductor memory structure coupled to said processor, said semiconductor memory structure comprising: a digit line [D] and a digit complement line [D*]; a circuit for precharging [24] said digit line and said digit complement line to a predetermined voltage [DVC2] value prior to a read operation; an access transistor [50] for coupling a programmable conductor memory element [54] to said digit line during a read operation; and a sense

amplifier [0] for comparing voltages on said digit line and said digit complement line during said read operation to determine a logical state of said memory element [see *the 2nd paragraph of the "Background of the Invention" section]*.

With respect to claim 514, Cowles et al. discloses that the predetermined voltage is approximately Vdd [DVC2]. It is interpreted that Vdd is just a designated label without any numerical value associated to it.

9. Claim 57 is rejected, as understood, under 35 U.S.C 102(e) as being anticipated by Cowles et al. [U.S. Patent #6,449,203].

With respect to claim 57, Cowles et al. discloses a method for reading a semiconductor memory cell, the method comprising: precharging [via 24] a digit line [D] and a digit complement line [D*] to a predetermined voltage value [DVC2]; activating an access transistor [50] coupled between an element [54] and said digit line to apply a read voltage to said element; and comparing the voltage on said digit line with a voltage on said digit complement line to determine a logical state of said element [see *the 2nd paragraph of the "Background of the Invention" section]*.

Allowable Subject Matter

10. Claims 14-32, 40-49, and 56 are allowable over the prior art of record.

11. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) a method for reading a semiconductor memory cell, the method

comprising: charging a first terminal of an access transistor of a cell and a reference conductor to a second predetermined voltage, wherein said first terminal is coupled to a column line of said cell, wherein a second terminal of said transistor is coupled to a second portion of a resistive element, and wherein said first terminal and said reference conductor are coupled to respective inputs of a comparator; and comparing a voltage at said first terminal with said second predetermined voltage a predetermined period of time after an act of discharging begins in order to determine a logical state of said cell.

Conclusion

12. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (703) 308-4838. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

14. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Michael T. Tran
Art Unit 2818
June 11, 2003